

## REMARKS

This is intended as a full and complete response to the Final Office Action dated October 21, 2002, having a shortened statutory period for response set to expire on January 21, 2002. Claims 1-24 are pending and stand rejected. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-3 and 11-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,076,205 to *Vowles, et al.* and further in view of U.S. Patent No. 6,022,185 to *Mokuo*.

Claims 4, 5, 7, 9 and 13-19, 21-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Vowles, et al.* and *Mokuo* as applied to claims 1-3 above, and further in view of U.S. Patent No. 5,611,861 to *Higashi*.

Claims 6, 10 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Vowles, et al.*, *Mokuo* and *Higashi* as applied to claims 4, 5 7 and 9 above, and further in view of U.S. Patent No. 4,854,611 to *Press*.

Applicants have amended the base claims to more clearly recite aspects of the invention, obviating the rejections. More specifically, Applicants have amended the base claims to include the limitation that the first and second chambers are disposed on a common side of a transfer chamber and that the second chamber is adjustable relative to the robot arms so that the robot can position the wafers with a preselected degree of accuracy onto the respective platforms for efficient processing of the wafers.

The references, neither alone nor in combination, teach, show, or suggest the claimed invention, as amended. Applicants submit that these amendments do not constitute new matter and do not necessitate a new search. Accordingly, entry of these amendments is respectfully requested.

PATENT

Atty. Dkt. No. APPM/5320/DCVD/JW

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

1. (Amended) Apparatus for processing multiple semiconductor wafers, the apparatus comprising:

a transfer chamber;

a first processing chamber mounted in fixed relation to the transfer chamber and having a first wafer-holding platform with a center;

a second processing chamber mounted in adjustable relation to the transfer chamber and to the first chamber and having a second wafer-holding platform with a center, wherein the first and second processing chambers are disposed on a common side of the transfer chamber; and

a robot rotatably mounted within the transfer chamber and having first and second wafer-holding arms [spaced] configured parallel to each other for inserting a pair of wafers simultaneously into the first and second chambers and for placing the wafers accurately centered over the respective platforms, the [spacing] second chamber is adjustable relative to the [spacing of the] robot arms such that the wafers are centered and placed with a preselected degree of accuracy onto the respective platforms for efficient processing of the wafers.

3. (Amended) Apparatus for processing multiple semiconductor wafers, the apparatus comprising:

a transfer chamber;

a first processing chamber mounted in known relation to the transfer chamber and having a first wafer-holding platform with a center;

a second processing chamber having a second wafer-holding platform with a center, wherein the first and second processing chambers are disposed on a common side of the transfer chamber;

a mechanism for adjustably mounting the second chamber in relation to the first chamber and to the transfer chamber, the mechanism providing a plurality of position adjustments for the second chamber; and

a robot rotatably mounted within the transfer chamber and having first and second wafer-holding arms [spaced] configured parallel to each other for inserting a pair of wafers simultaneously into the first and second chambers and for placing the wafers accurately centered over the respective platforms, the [spacing] second chamber is adjustable relative to the [spacing of the] robot arms such that the wafers are centered and placed with a preselected degree of accuracy onto the respective platforms for efficient processing of the wafers.

7. (Amended) Apparatus for processing at least two semiconductor wafers simultaneously, the apparatus comprising:

a transfer chamber;

a load-lock chamber adjacent the transfer chamber;

a first processing chamber mounted in known relation to the transfer chamber and having a first wafer-holding platform with a center;

a second processing chamber having a second wafer-holding platform with a center, wherein the first and second processing chambers are disposed on a common side of the transfer chamber;

adjusting means for adjustably mounting the second chamber in relation to the first chamber and to the transfer chamber, the adjusting means having a bellows assembly positioned between the transfer chamber and the second chamber and providing for relative movement thereof and also providing a wafer passageway between the chambers while maintaining an hermetic seal; and

a robot rotatably mounted around a center axis within the transfer chamber and having first and second wafer-holding arms [spaced] configured parallel to each other for withdrawing a pair of wafers from the load-lock chamber and inserting the pair of wafers simultaneously into the first and second chambers and for positioning both of the wafers with a preselected degree of accuracy over the respective platforms, the [spacing of the platform centers] second chamber is adjustable [to the preselected degree of accuracy by the adjusting means] relative to [each other and to the spacing of] the robot arms and the center axis such that the wafers are centered and placed with

the preselected degree of accuracy onto the respective platforms for efficient processing of the wafers.

9. (Amended) Apparatus for processing a pair of semiconductor wafers simultaneously, the apparatus comprising:

a transfer chamber;

a load-lock chamber adjacent the transfer chamber;

a first processing chamber mounted in fixed relation to the transfer chamber and having a first wafer-holding platform with a center;

a second processing chamber having a second wafer-holding platform with a center, wherein the first and second processing chambers are disposed on a common side of the transfer chamber;

mechanical means for adjustably mounting the second chamber in relation to the first chamber and to the transfer chamber; the mechanical means supporting the second chamber against the transfer chamber in cantilever fashion and having a bellows assembly positioned between the transfer chamber and the second chamber to provide for relative movement thereof and to provide a wafer passageway between the respective chambers while maintaining an hermetic seal;

a slit valve adjacent the passageway for hermetically sealing the transfer chamber from the second chamber; and

a remotely controlled robot rotatably mounted around a center axis within the transfer chamber and having first and second wafer-holding arms [spaced] configured parallel to each other for withdrawing a pair of wafers from the load-lock chamber and inserting the pair of wafers simultaneously into the first and second chambers and for positioning both of the wafers to a preselected degree of accuracy over the respective platforms, the [spacing of the platform centers] second chamber is adjustable by the mechanical means relative to [each other and to the spacing of] the robot arms and the center axis such that the wafers are centered and placed with the preselected degree of accuracy onto the respective platforms for efficient processing of the wafers.

11. (Amended) An apparatus for processing multiple semiconductor wafers, comprising:

a transfer chamber;

at least one pair of processing chambers disposed about the transfer chamber, wherein each pair of processing chambers comprises:

a first processing chamber mounted in known relation to the transfer chamber;

and

a second processing chamber adjustably mounted to the transfer chamber, wherein the first and second processing chambers are disposed on a common side of the transfer chamber;

a mechanism for positioning the second processing chamber in relation to the first processing chamber and in relation to the transfer chamber; and

a robot mounted within the transfer chamber for inserting a pair of wafers simultaneously into the first and second processing chambers.

17. (Amended) An apparatus for processing multiple semiconductor wafers, comprising:

a transfer chamber;

at least one pair of processing chambers disposed about a common side of the transfer chamber, wherein each pair of processing chambers comprises:

a first processing chamber disposed in known relation about the transfer chamber; [and]

a second processing chamber adjustably disposed about the transfer chamber; and

a bellows assembly disposed between the second processing chamber and the transfer chamber; and

a robot mounted within the transfer chamber adapted to insert a pair of wafers simultaneously into the first and second processing chambers.

24. (Amended) An apparatus for processing multiple semiconductor wafers, comprising:

a transfer chamber;

at least one pair of processing chambers disposed about a common side of the transfer chamber, wherein each pair of processing chambers comprises:

a first processing chamber disposed in known relation about the transfer chamber; [and]

a second processing chamber adjustably disposed about the transfer chamber; and

a bellows assembly disposed between the second processing chamber and the transfer chamber; and

a robot having horizontal arms and mounted within the transfer chamber for inserting a pair of wafers simultaneously into the first and second processing chambers, the robot having at least two arms extendable along respective longitudinal, parallel axes.